WHAT IS CLAIMED IS:

1. A programmable, low gate latency, system-on-chip embedded processor system for supporting general input/output applications, comprising:

a modular, multiple bit, multithread processor core operable by at least four parallel and independent application threads sharing common execution logic segmented into a multiple stage processor pipeline, wherein said processor core is capable of having at least two states;

a logic mechanism engaged with said processor core for executing an instruction set within said processor core to generate instruction state data;

a supervisory control unit, controlled by at least one of said processor core threads, for examining said core processor state and for controlling said core processor operation;

at least one memory for storing and executing said instruction set data and for storing system values; and

a peripheral adaptor engaged with said processor core for transmitting input/output signals to and from said processor core.

2. A system as recited in Claim 1, wherein stages of said pipeline are capable of breaking each instruction decode operation into multiple sub-processing steps within a logic chain.

3. A system as recited in Claim 2, further comprising a minimal number of gates in a logic chain to reduce the effects of gate latency.

4. A system as recited in Claim 1, wherein said processor logic and system memory are constructed from substantially the same integrated circuit process technology.

5. A system as recited in Claim 1, further comprising a clock adaptor mechanism for connecting an internal clock to an external crystal frequency, wherein the internal clock frequency is adjusted from said external crystal frequency and wherein said internal clock frequency can be changed dynamically by a processor thread so said internal clock operates at different frequencies than an external crystal frequency.

6. A system as recited in Claim 5, wherein a setting to control the internal clock rate is stored in nonvolatile memory.

7. A system as recited in Claim 6, wherein at least one memory is of a nonvolatile external type in which system settings may be stored by an external testing apparatus.

8. A system as recited in Claim 5, wherein said processor internal clock frequency is programmed to be different than said external crystal frequency to compensate for external crystal operating frequency variations.

9. A system as recited in Claim 5, wherein said processor internal clock frequency is programmed to be different than the external crystal frequency to synchronize the internal processor clock frequency with a derived clock frequency from a peripheral input signal.

10. A system as recited in Claim 1, further comprising a clock adaptor mechanism external to and programmable by said processor core through digital outputs controlled by said processor core.

11. A system as recited in Claim 1, further comprising a watchdog mechanism implemented by at least one thread checking the status of at least one other system thread through a state record updated by the checked thread and read by the checking threads.

12. A system as recited in Claim 11, wherein said checking to checked thread association is statically defined.

13. A system as recited in Claim 11, wherein said checking to checked thread association is a dynamic relationship governed by an algorithm.

14. A system as recited in Claim 11, wherein a checking thread can alter the operation of a checked thread following identification of an unacceptable state record.

15. A system as recited in Claim 11, wherein a checking thread can reset said processor core following identification of an unacceptable state record.

16. A system as recited in Claim 1, wherein any of the processor threads can be disabled by said processor core to conserve power.

17. A system as recited in Claim 5, wherein said processor clock frequency can be altered by any of the processor threads to conserve power.

18. A system as recited in Claim 1, wherein said supervisory control unit is capable of changing the core processor operation to provide power management function.